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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/045,297	11/07/2001	Dongyun Lee	594728112US	1257

25096 7590 11/21/2006

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EXAMINER	
KIM, HONG CHONG	
ART UNIT	**PAPER NUMBER**
2185	

DATE MAILED: 11/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/045,297	LEE ET AL.	
	Examiner	Art Unit	
	Hong C. Kim	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) *37-40* is/are withdrawn from consideration.

5)☒ Claim(s) *4 and 23* is/are allowed.

6)☒ Claim(s) *1-3,5-22 and 24-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *37-40* are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-40 are presented for examination. This office action is in response to the RCE filed on 9/20/06.

2. This is an RCE of applicant's earlier Application No. 10/045297. All claims are drawn to the same invention claimed in the earlier application and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the earlier application. Accordingly it would appear a first action FINAL would be appropriate in this case, even though it is a first action in this case. See MPEP § 706.07(b).

The more than 2 months since the RCE was filed is deemed more than adequate time in which to consider and prepare a response or preliminary amendment.

Nevertheless, this action is NOT being made final in order to provide applicants more latitude in amending the claims to overcome the outstanding rejections in hope of expediting prosecution of this application. Applicants' cooperation in reducing or removing the issues involved in this case so that prosecution may be expedited to allowance, appeal, or abandonment is respectively solicited.

Restriction

3. Newly submitted claim 37-40 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: it appears that added claims 37-40, drawn to classified in class 375, subclass 286.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claim 37-40 withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Specification

4. Applicants are requested to update the status of the related U.S. patent application accordingly (e.g., U.S. Patent Application Serial No. ##/###,### filled Sept. 07, 1990, now abandoned; ..., now U.S. Patent #,###,### issued Jan. 01, 1994; or This application is a continuation of Serial Number ##/###,###, filed on December 01, 1990, now abandoned; ...etc.). Also applicants are requested to include the status of the related U.S. applications or patents in the CROSS-REFERENCE TO RELATED APPLICATIONS section and in any other corresponding area in the specification, if any.

5. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The title should be more specific to differentiate the invention from similar inventions in the patent literature. The "serial comm" "plesiosynchronous without a clock", "in-band symbols for data", and "out of band symbols for control" aspects of the invention should be mentioned in the title so that the title is more descriptive.

Drawings

6. Applicant is requested to particularly point out the figure number(s) in the submitted drawings that is specifically directed to the claimed invention.

Information Disclosure Statement

7. Applicants are reminded of the duty to disclose information under 37 CFR 1.56.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1, 2, 5-7, 8, 10-21 and 24-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sonnier et al (US 5,574,849) and Davidson et al (US 6,826,199) and Knecht et al (US 5,592,487),

As per claim 1, Sonnier discloses a memory device comprises a memory *[memory 28;* Fig. 2]; and a plurality of ports for accessing the memory of the memory device *[ports o-5 of router 14 and X and Y ports of CPU 12;* Figs. 1 A, 1 B], each port having a bit serial communications link for receiving from and transmitting to an accessing device *[TNet links* LA *connecting routers 14A and 14s;* Fig. 1 B], each port using plesiosynchronous technique to receive symbols and using in-band symbols to

transmit data *[command/data symbols to be transmitted out of X and Y encoders;* col. 27, lines 30-38; *T_clock and Rcv clock are of the* same *frequency;* col. 68, lines 62-65; *the clock* signal *accompanies the symbol stream;* col. 68, lines 47-50]; and out-of-band symbols to transmit control information *[Y encoder transmits IDLE symbols or other* symbols *used to perform control functions;* col. 28, lines 31-35].

However, Sonnier does not specifically teach using a plesiosynchronous technique without transmitting a clock signal and the bits of each symbol are received and transmitted serially as recited in the claim.

Davidson discloses a bit stream having an inherent clock or plesiochronous clock that is neither synchronous nor asynchronous (column 1, lines 28-30) thereby providing the ability to switch separate, incoming traffic streams carrying data at different rates without affecting the clock (column 1, lines 14-16, 58-59).

Regarding claim 1, it would have been obvious to one of ordinary skill in the art, at the time of invention by applicant to modify the system of Sonnier to include using a plesiosynchronous technique without transmitting a clock signal in the system of Sonnier because it was well known to provide the ability to switch separate, incoming traffic streams carrying data at different rates (column 1, lines 14-16, 58-59) as taught by Davidson.

Knecht discloses serially receiving and transmitting bits of each symbol (column 7, lines 37-42).

Further regarding claim 1, it would have been obvious to one of ordinary skill in the art, at the time of invention by applicant to modify the system of Sonnier and

Davidson to include serially receiving and transmitting bits of each symbol in order to provide a high speed serial data transfer requiring minimal overhead (column 1, lines 65-67) as taught by Knecht.

As per claim 19, Sonnier discloses a memory device comprising: a memory that reads and writes data *[memory 2s;* Fig. 2]; a multiphase clock generator that provides a multiphase clock signal *[clock generator 654;* Figs. 24 and 25; *phase comparator 660 detects a phase difference;* col. 67, lines 17-29]; and a plurality of ports *[ports 0-5 of router 94 and X and Y ports of CPU 12;* Figs. 1A, 1 B], each port for connecting to a serial communications link and for receiving data and control information via the serial communications link using a plesiosynchronous technique *[command/data symbols to be transmitted out of X and Y encoders;* col. 27, lines 30-38; *Y encoder transmits IDLE symbols or other symbols used to perform control functions;* col. 28, lines 31-35; *T_clock and Rcv clock are of the same frequency;* col. 68, lines 62-65], wherein each port uses the generated multiphase clock signal generated by the multiphase clock generator *[clock oscillator 652 is used for developing the M_clock signal for both CPUs 12;* col. 67, lines 40-59].

However, Sonnier does not specifically teach using a plesiosynchronous technique without transmitting a clock signal and the bits of each symbol are received and transmitted serially as recited in the claim.

Davidson discloses a bit stream having an inherent clock or plesiochronous clock that is neither synchronous nor asynchronous (column 1, lines 28-30) thereby providing

the ability to switch separate, incoming traffic streams carrying data at different rates without affecting the clock (column 1, lines 14-16, 58-59).

Regarding claim 19, it would have been obvious to one of ordinary skill in the art, at the time of invention by applicant to modify the system of Sonnier to include using a plesiosynchronous technique without transmitting a clock signal in the system of Sonnier because it was well known to provide the ability to switch separate, incoming traffic streams carrying data at different rates (column 1, lines 14-16, 58-59) as taught by Davidson.

Knecht discloses serially receiving and transmitting bits of each symbol (column 7, lines 37-42).

Further regarding claim 19, it would have been obvious to one of ordinary skill in the art, at the time of invention by applicant to modify the system of Sonnier and Davidson to include serially receiving and transmitting bits of each symbol in order to provide a high speed serial data

As per claim 20, Sonnier discloses data is sent using in-band symbols *[command/data symbols to be transmitted out of X and Y encoders;* col. 27, lines 30-381; and control information is sent via out-of-band symbols *[Y encoder transmits IDLE symbols or other symbols used to perform control functions;* col. 28, lines 31-35].

As per claims 2 and 21, Sonnier discloses each serial communications link is connected to an accessing device via a point-to-point connection [*Tnet links LA*

connecting routers 14A and 14B are directly connected from one port *to the other;* Fig. 1 B].

As per claims 5 and 24, Sonnier discloses the memory includes multiple banks and wherein multiple banks can be simultaneously accessed by different ports [*Mcs 26a and 26b run in parallel to provide a path between the memory array and the interfaces 24a, 24b; and one Mc is connected to simultaneously access consecutive even addresses;* Fig. 2; col. 46, lines 7-22].

As per claims 6 and 25, Sonnier discloses each bank includes multiple sections and wherein multiple sections can be simultaneously accessed by different ports *[one Mc is connected to simultaneously access consecutive even addresses; the other Mc is similarly connected to access odd addresses;* Fig. 16; col. 46, lines 23-35].

As per claims 7 and 26, Sonnier discloses multiple sections and wherein multiple sections can be simultaneously accessed by different ports *[one Mc is connected to simultaneously access consecutive even addresses; the other Mc is similarly connected to access odd addresses;* Fig. 16; col. 46, lines 23-35].

As per claims 8 and 27, Sonnier, discloses the multiple sections are configurable on a port-by-port basis *[establishing redundant communication paths between any CPUs 12, router 14A', in* port *4, out* port *3;* col. 13, lines 19-34].

As per claim 28, Sonnier discloses the memory device of claim 27 including the configuration information storage *[ports 4 and 5 may vary from the other ports 0-3 of the router 14;* col. 6-11].

As per claims 10 and 29, Sonnier discloses the ports are connected to the memory using time-division multiplexing *[incoming symbols are buffered and passed to MUX 104;* col. 22, lines 22-30; *each symbol is clocked out and passed to the storage and processing units by MUX 104;* col. 25, lines 2-13].

As per claims 11 and 30, Sonnier discloses the ports are connected to the memory using a crossbar switch *[the routers provide a cross-link path from one end to the other;* Fig. 1A; col. 12, lines 12-28].

As per claims 12 and 31, Sonnier discloses control information is transmitted as a primitive *[X and Y encoders transmit IDLE: symbols or other symbols to perform control functions;* col. 28, lines 31-35].

As per claims 13 and 32, Sonnier discloses a primitive includes two out-of-band symbols *[both X and Y encoders transmit IDLE symbols or other symbols to perform control functions;* col. 28, lines 31-35].

As per claims 14 and 33, Sonnier discloses control information includes a synchronization symbol *[SYNC command symbol;* col. 26, lines 18-35].

As per claims 15 and 34, Sonnier discloses the plesiosynchronous technique includes inserting or removing symbols to compensate for variations between clock frequencies of the accessing device and the memory device *[a constant stream of symbols is always being transmitted from all ports;* col. 24, lines 8-61].

As per claim 16, Sonnier discloses the ports share a single multiphase clock generator *[clock generator 654;* Fig. 24; *c01.* 67, lines 1-13].

As per claims 17 and 35, Sonnier discloses the multiphase clock generator is a phase lock loop *[all clock signals are phase-locked to M_Clk;* col. 67, lines 12-14].

As per claims 18 and 36, Sonnier discloses a synchronization symbol encodes a memory command *[command symbols communicates between various CPUs and I/O packets interfaces. Simplifying design, the processor will construct a data structure in memory;* col. 16, lines 39-53].

9. Claims 3 and 22 are rejected under 35 U.S.C. 103(x) as being unpatentable over Sonnier et al (US 5,574,849) and Davidson et al (US 6,826,199) and Knecht et al (US 5,592,487) and Jeong et al (US 6,229,859).

As per claims 3 and 22, Sonnier and Davidson and Knecht disclose the claimed invention as detailed above in the previous paragraphs. However, Sonnier and Davidson and Knecht do not specifically teach oversampling data as recited in the claims.

Jeong discloses oversampling data for the purpose of synchronizing the operation of the receiver's clock signal with that of the transmitter (col. 3, lines 49-56).

However, oversampling data is well known in the art for generating an oversampled data stream for the purpose of synchronizing the operation of the receiver's clock signal with that of the transmitter as evidenced by Jeong.

Since the technology for oversampling data was well known and since oversampling data synchronizes the operation of the receiver's clock signal with that of the transmitter, an artisan would have recognized the advantage of oversampling data as taught by Jeong in the system of Sonnier.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to apply Jeong's teaching of oversampling data because it was well known to synchronize the operation of the receiver's clock signal with that of the transmitter as taught by Jeong.

10. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sonnier et al (US 5,574,849) and Davidson et al (US 6,826,199) and Knecht et al (US 5,592,487) and Lee (US 5,307,314).

As per claim 9, Sonnier discloses the claimed invention as detailed above in the previous paragraphs. However, Sonnier does not specifically teach configuration information enabling certain sections of the bank as recited in the claim.

Lee discloses configuration information enabling certain sections of a bank is well known in the art for the purpose of allowing a split read/write operation of parallel read and write sections (col. 8, lines 30-38).

However, configuration information enabling certain sections of a bank is well known in the art for the purpose of allowing a split read/write operation of parallel read and write sections as evidenced by Lee.

Since the technology for implementing configuration information enabling certain sections of a bank was well known and since configuration information enabling certain sections of the bank allows a split read/write operation of parallel read and write sections, an artisan would have recognized the advantage of implementing configuration information enabling certain sections of the bank as taught by Lee in the system of Sonnier.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to apply Lee's teaching of configuration information enabling certain sections of the bank because it was well known to allow a split read/write operation of parallel read and write sections as taught by Lee.

Allowable Subject Matter

11. Claims 4 and 23 are allowed over the prior art of record.

Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See attached PTO-892.

2. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

3. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. ' 1.111(c).

4. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hong C Kim whose telephone number is (571) 272-4181. The examiner can normally be reached on M-F 9:00 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 whose telephone number is (571) 272-2100.

6. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

7. **Any response to this action should be mailed to:**

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

or faxed to TC-2100:
(571)-273-8300

Hand-delivered responses should be brought to the Customer Service Window (Randolph Building, 401 Dulany Street, Alexandria, VA 22314).

HK

Primary Patent Examiner
November 18, 2006